วงจรจำลองฟังก์ชันอิมมิตแตนซ์แบบลอยตัวที่สามารถปรับค่าได้อย่างง่าย โดยปราศจากตัวต้านทานภายนอก

Simple Topology of Tunable Floating Immittance Function Simulators without External Resistor

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บทคัดย่อ

บทความนี้นำเสนอวงจรจำลองอิมมิตแตนซ์แบบลอยตัวโดยใช้วงจรคอนดักเตอร์และตัวเก็บประจุแบบลงกราวนด์ต่อร่วมกันเท่านั้น โดยวงจรที่นำเสนอมีจุดเด่น คือ มีวงจรเรียบง่าย ปราศจากตัวต้านทานภายนอกและใช้จำนวนอุปกรณ์ในแต่ละวงจรน้อย รวมถึงสามารถปรับค่าพารามิเตอร์ของวงจรได้ด้วยวิธีการทางอิเล็กทรอนิกส์ด้วยการปรับกระแสไบอัสของวงจรทรานสคอนดักเตอร์ ผลการจำลองการทำงานของวงจรที่เสนอและการประยุกต์ใช้งานโดยใช้เทคโนโลยีของทรานซิสเตอร์ชนิดซีมอส 0.18 μm ได้ยืนยันสมรรถนะของวงจรด้วย

Abstract

This article presents a simple way of configuring the floating immittance function simulators based on transconductors and only grounded capacitors is presented. The proposed circuits offer some key features are simple circuit layout, which is the result of using less components and lastly, external resistors are not required for these circuits. Furthermore, the parameter of the proposed circuits can be electronically adjusted by changing the bias current of the transconductors. Some simulation results of the circuits and theirs applications using 0.18 μm CMOS transistor process are presented to verify the circuit performances.

1. Introduction

Passive elements i.e. inductor, capacitor and resistor are necessary components in analog circuit applications such as filters, oscillators, sensors, impedance matching circuits and element cancellation circuits, to name a few. However, the large-value passive element is a main drawback of integrated circuit fabrication because of its large occupation of chip area. To abstain from this drawback, the realization of an immittance function simulator circuit using active building blocks (ABBs) to replace the bulky passive element. In recent years, several circuits of the immittance function simulators have been reported in the literature [1 - 10]. In [1, 4], a grounded capacitance multiplier based on two current feedback

operational amplifiers (CFOAs), two resistors and a capacitor is presented. The configuration of grounded capacitance / resistance simulator employing a CFOA, two operational transconductance amplifiers (OTAs) and a passive element have been proposed in [2]. A circuit of two OTAs, a dual output second generation current conveyor (CCII±) and a passive element simulates a floating capacitance / resistance multiplier [3]. In [5], a grounded capacitance multiplier consists of two current follower transconductance amplifiers (CFTAs) and three passive elements. In [6], the configuration of floating immittance simulator (inductance, capacitance and resistance) using two differential voltages to current converters (DVTCs) and three passive components is reported; while the floating simulator of [7] requires two current conveyor transconductance amplifiers (CCTAs), four MOS switches, one MOS resistor and two circuit components (a floating capacitor / one MOS resistors or two MOS resistors). A floating capacitance multiplier employing a dual output second generation voltage conveyor (VCII±), an electronically tunable differential voltage current conveyor (E-DVCC) and a grounded capacitor is presented in [8]. In [9], a circuit of three VCIIs and a grounded capacitor provides a floating inductance simulator. The circuits of a floating frequency dependent negative conductance (FDNC) using two voltage differencing transconductance amplifiers (VDTAs) and two capacitors and a grounded frequency dependent negative resistance (FDNR) are reported in [10]. However, these proposed immittance simulators in the literature possess one or more of the following drawbacks:

(i) Only grounded immittance simulator [1, 2, 4, 5]. In numerous applications, floating immittance simulator is more flexible and versatile than the grounded ones.

(ii) Use of capacitor connection to X terminal of ABB such as CFOA, CCII and VCII [2, 3, 8, 9], it degrades the performance of immittance simulator owing to parasitic resistance at X terminal of the ABB.

(iii) Use of floating passive component [1, 4, 5, 6, 7] and external resistor [1 - 7].

(iv) Use of excessive number of transistors [5-10]. The cases of (iii) and (iv) require large dimension of chip. So, there are not attractive for integrated circuit implementation.

This paper is thus focused on the study of the simple topology of floating immittance function simulator circuits. The proposed simulator circuits employ some simple transconductors and only grounded capacitor without external resistor. Depending on the

option of circuit configuration, the proposed circuits can simulate resistor, inductor, capacitor, FDNR and FDNC. They are suitable for integrated circuit fabrication. To confirm the performances of proposed circuits, various SPICE simulations are exhibited. In Table 1, the comparison of the proposed circuits and several prior works are shown.

Table 1 Comparison of the immittance function simulator.

Ref.	Active components	Type of simulator	Floating/ Ground	Floating passive component	External resistor	Electronic tunning	Supply voltage
[1]	2 CFOAs	- C	Ground	Yes	Yes	No	±10 V
[2]	1 CFOA 2 OTAs	- C - R	Ground	No	Yes	Yes	±5 V
[3]	1 CFOA 2 OTAs	- C - R	Floating	No	Yes	Yes	-
[4]	2 CFOAs	- C	Ground	Yes	Yes	No	±9 V
[5]	2 CFTAs (54 MOSs)	- C	Ground	Yes	Yes	Yes	±0.75 V
[6]	2 DVTCs (32 MOSs)	- C - L - FDNR	Floating	Yes	Yes	No	±0.75 V
[7]	2 CCTAs (46 MOSs)	- C - L - R	Floating	Yes	Yes	Yes	±1.2 V
[8]	1 VCII±, 1 E-DVCC (46MOSs)	- C	Floating	No	No	Yes	±0.9 V
[9]	3 VCIIs (51 MOSs)	- L	Floating	No	No	Yes	±0.9 V
[10]	2 VDTAs (36 MOSs)	- FDNC	Floating	No	No	Yes	±0.9 V
This work	2 transconductors (8 MOSs)	- L	Floating	No	No	Yes	±0.75 V
	4 transconductors (16 MOSs)	- C	Floating	No	No	Yes	±0.75 V
	3 transconductors (12 MOSs)	- FDNC	Floating	No	No	Yes	±0.75 V
	5 transconductors (20 MOSs)	- FDNR	Floating	No	No	Yes	±0.75 V
	1 transconductor (4 MOSs)	- R	Floating	No	No	Yes	±0.75 V

2. Proposed Floating Immittance Function Simulator Description

In this section, the description of basic proposed circuit topology, proposed immittance function simulator circuits and theirs parasitic element effect consideration are presented. The details of them are as follows:

2.1 Basic Proposed Circuit Topology

In the proposed immittance simulator, the simple transconductor is mainly used as ABB, its property is shortly reviewed. The transconductor choosing four CMOS transistors and two current sources is presented in Figure 1 [11]. Assuming that four CMOS transistors of the transconductor operate in the saturation region and theirs transconductances are equal. The current output of the transconductor follows as

$$I_p = -I_n = g_m(V^+ - V^-), \quad (1)$$

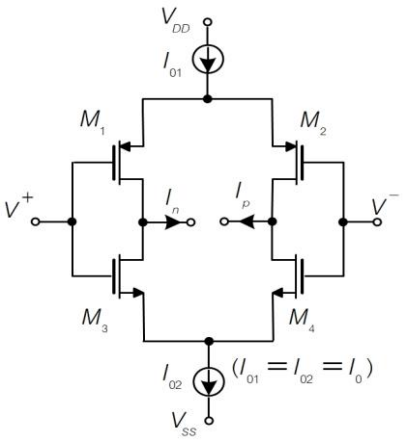

Figure 1 Simple transconductor.

where g_m is the transconductance of the transistor of transconductor, it is shown as

$$g_m = (\mu_0 C_{ox} \frac{W}{L} I_0)^{\frac{1}{2}}, \quad (2)$$

where the parameters of μ_0, C_{ox} and *W/L* are the carrier mobility, the oxide capacitance and aspect ratio of the CMOS transistor, respectively. I_0 is the bias current of the transconductor.

The basic topology for realizing the proposed floating immittance simulator is shown in Figure 2 (a), its equivalent circuit is displayed in Figure 2 (b). The topology consists of a simple transconductor and a current transfer function block, T(s). Since $I_1 = -I_2 = T(s)I_x$, routine analysis of the topology gives the admittance matrix as

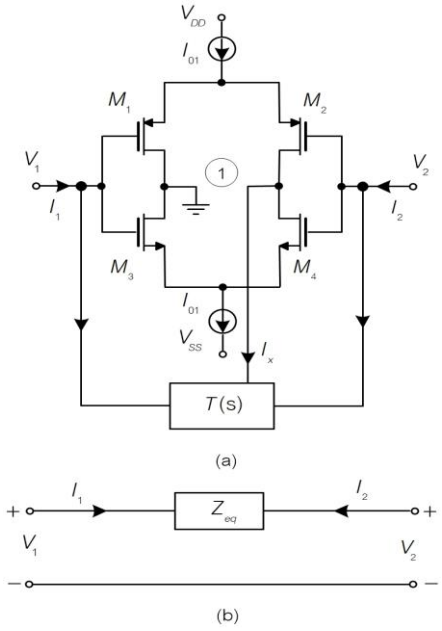

Figure 2 (a) Basic proposed circuit topology,
(b) Equivalent circuit of Figure 1 (a).

$$\mathbf{Y} = \frac{1}{Z_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} = g_m T(s) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}. \quad (3)$$

From (3), the topology can be used for converting the current transfer function T(s) into the floating immittance function simulator, where the impedance function can be expressed as

$$Z_{eq} = \frac{1}{g_{m1} T(s)}, \quad (4)$$

where g_{m1} is the transconductance of the first transconductor. The details of the proposed circuits using the topology are described in next section.

2.2 Proposed Circuits

From Figure 2 (a), depending on the selection of *T(s)*, the floating inductor, capacitor, FDNR, FDNC and resistor can be simulated as follows:

(i) If integrator transfer function of $T(s) = g_{m2} / sC_1$ is selected, the floating inductor is presented in Figure 3, its impedance is expressed as

$$Z_{eq} = sL_{eq} = s\frac{C_1}{g_{m1} g_{m2}}, \quad (5)$$

where $L_{eq} = C_1 / g_{m1} g_{m2}$.

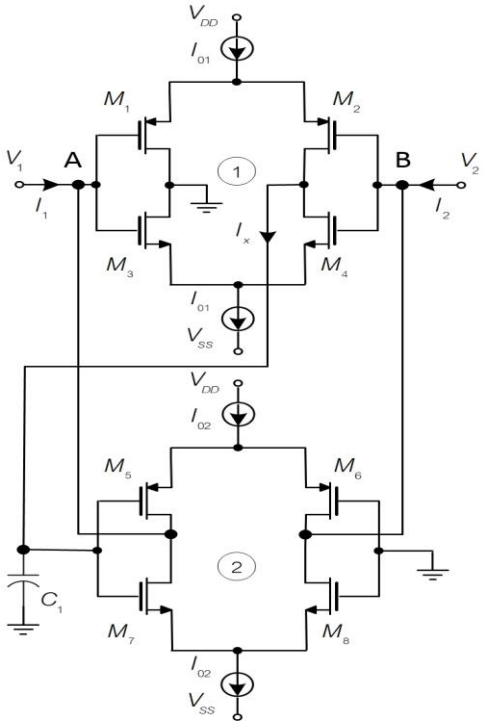

Figure 3 Floating inductor.

(ii) If differentiator transfer function of $T(s) = sg_{m3} C_1 / g_{m2} g_{m4}$ is selected, the floating capacitor is shown in Figure 4, its impedance is expressed as

$$Z_{eq} = \frac{1}{sC_{eq}} = \frac{g_{m2} g_{m4}}{sg_{m1} g_{m3} C_1}, \quad (6)$$

where $C_{eq} = g_{m1} g_{m3} C_1 / g_{m2} g_{m4}$.

(iii) If transfer function of $T(s) = g_{m2} g_{m3} / s^2 C_1 C_2$ is selected, the floating FDNC (super inductor) is presented in Figure 5, its impedance is manifested as

$$Z_{eq} = s^2 M_{eq} = s^2 \frac{C_1 C_2}{g_{m1} g_{m2} g_{m3}}, \quad (7)$$

where $M_{eq} = C_1 C_2 / g_{m1} g_{m2} g_{m3}$.

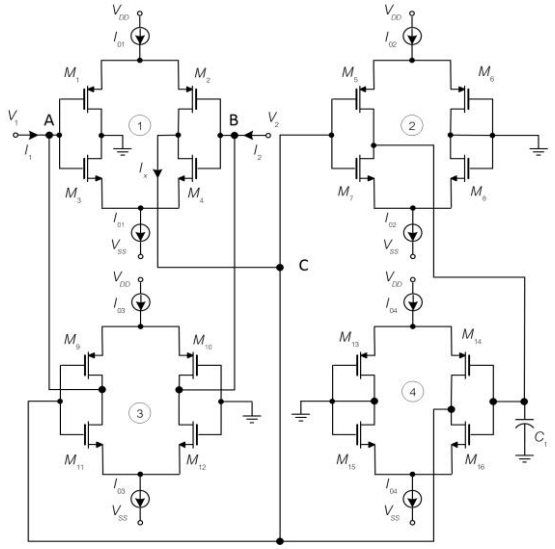

Figure 4 Floating capacitor.

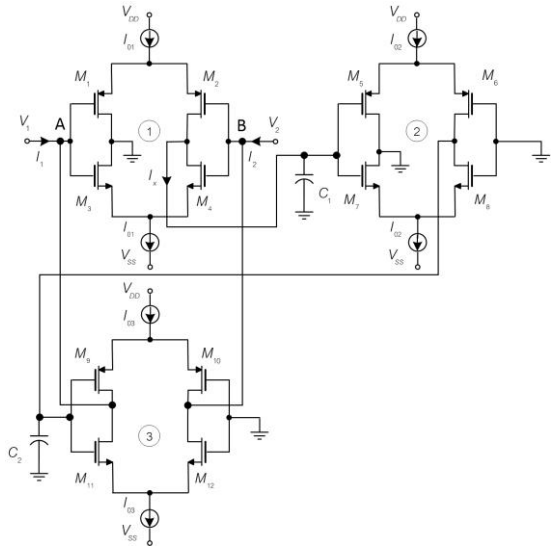

Figure 5 Floating FDNC.

(iv) If transfer function of $T(s)=s^2 g_{m3} C_1 C_2 / g_{m2} g_{m4} g_{m5}$ is selected, the floating FDNR is shown in Figure 6, its impedance is expressed as

$$Z_{eq} = \frac{1}{s^2 D_{eq}} = \frac{g_{m2} g_{m4} g_{m5}}{s^2 g_{m1} g_{m3} C_1 C_2}, \qquad (8)$$

where $D_{eq} = g_{m1} g_{m3} C_1 C_2 / g_{m2} g_{m4} g_{m5}$.

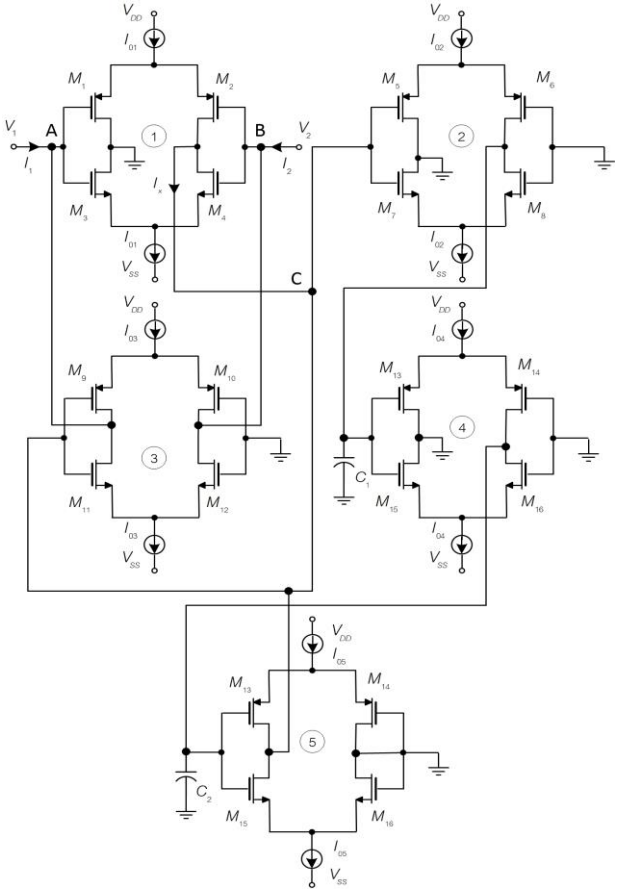

Figure 6 Floating FDNR.

(v) If transfer function of $T(s)=1$ is selected and the property of transconductor in Figure 1 is applied, the floating resistor is shown in Figure 7, its impedance is expressed as

$$Z_{eq} = R_{eq} = \frac{1}{g_{m1}}. \qquad (9)$$

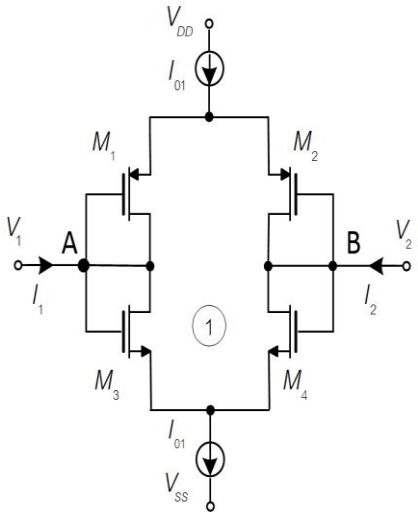

Figure 7 Floating resistor.

From (5)-(9), electronic tunability of these impedances can be adjusted by changing the g_{mi} via the bias current of i^{th} transconductor. The impedance of each proposed circuits can be modified independently. Moreover, the sensitivities of the impedance of the proposed circuits with respect to circuit components give the acceptable low values, they are found to be:

$$S_{C_1}^{L_{eq}} = S_{C_1,g_{m1},g_{m3}}^{C_{eq}} = S_{C_1,C_2}^{M_{eq}} = S_{C_1,C_2,g_{m1},g_{m3}}^{D_{eq}} = 1, \quad (10)$$

$$S_{g_{m1},g_{m2}}^{L_{eq}} = S_{g_{m2},g_{m4}}^{C_{eq}} = S_{g_{m1},g_{m2},g_{m3}}^{M_{eq}} = -1, \quad (11)$$

and

$$S_{g_{m2},g_{m4},g_{m5}}^{D_{eq}} = S_{g_{m1}}^{R_{eq}} = -1. \quad (12)$$

It is noted that the negative impedance of the proposed circuits can be produced by interchangeable connection between node A and node B of the circuits of Figures 3 – 7.

2.3 Parasitic Element Consideration

To present the parasitic element effects of transcoductor on the proposed circuits, the equivalent circuit of the transconductor with parasitic elements is shown in Figure 8, where C_+, C_-, C_P and C_N are the low-value capacitance and g_P and g_N are the low-value conductance.

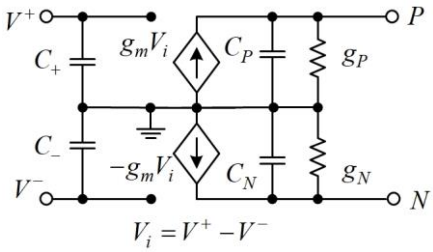

Figure 8 Equivalent circuit of transconductor with parasitic element.

Routine analysis of the proposed circuit in Figures 3 to 7 including the parasitic element of the transconductor yields in the following as

(i) Circuit of Figure 3 (inductor)

$$I_1 = \frac{g_{m1}g_{m2}}{y_{CT1}}(V_1 - V_2) + y_A V_1, \quad (13)$$

$$I_2 = -\frac{g_{m1}g_{m2}}{y_{CT1}}(V_1 - V_2) + y_B V_2, \quad (14)$$

where $y_A = g_{N2} + s(C_{+1} + C_{N2})$,

$y_B = g_{P2} + s(C_{-1} + C_{P2})$,

$y_{CT1} = g_{P1} + s(C_1 + C_{P1})$

(ii) Circuit of Figure 4 (capacitor)

$$I_1 = \frac{g_{m1}g_{m3}y_{CT1}}{g_{m2}g_{m4} + y_{CT1}y_C}(V_1 - V_2) + y_A V_1, \quad (15)$$

$$I_2 = -\frac{g_{m1}g_{m3}y_{CT1}}{g_{m2}g_{m4} + y_{CT1}y_C}(V_1 - V_2) + y_B V_2, \quad (16)$$

where $y_A = g_{N3} + s(C_{+1} + C_{N3})$,

$y_B = g_{P3} + s(C_{-1} + C_{P3})$,

$y_C = g_{P1} + g_{P4} + s(C_{P1} + C_{+2} + C_{+3} + C_{P4})$

$y_{CT1} = g_{N2} + s(C_1 + C_{N2} + C_{-4})$

(iii) Circuit of Figure 5 (FDNC)

$$I_1 = \frac{g_{m1}g_{m2}g_{m3}}{y_{CT1}y_{CT2}}(V_1 - V_2) + y_A V_1, \quad (17)$$

$$I_2 = -\frac{g_{m1}g_{m2}g_{m3}}{y_{CT1}y_{CT2}}(V_1 - V_2) + y_B V_2, \quad (18)$$

where $y_A = g_{N3} + s(C_{+1} + C_{N3})$,

$y_B = g_{P3} + s(C_{-1} + C_{P3})$,

$y_{CT1} = g_{P1} + s(C_1 + C_{P1} + C_{+2})$

$y_{CT2} = g_{P2} + s(C_2 + C_{P2} + C_{+3})$

(iv) Circuit of Figure 6 (FDNR)

$$I_1 = \frac{g_{m1}g_{m3}}{\frac{g_{m2}g_{m4}g_{m5}}{y_{CT1}y_{CT2}} + y_C}(V_1 - V_2) + y_A V_1, \quad (19)$$

$$I_2 = -\frac{g_{m1}g_{m3}}{\frac{g_{m2}g_{m4}g_{m5}}{y_{CT1}y_{CT2}} + y_C}(V_1 - V_2) + y_B V_2, \quad (20)$$

where $y_A = g_{N3} + s(C_{+1} + C_{N3})$,

$y_B = g_{P3} + s(C_{-1} + C_{P3})$,

$y_C = g_{P1} + g_{N5} + s(C_{P1} + C_{+2} + C_{+3} + C_{N5})$

$y_{CT1} = g_{P2} + s(C_1 + C_{P2} + C_{+4})$

$y_{CT2} = g_{P4} + s(C_2 + C_{P4} + C_{+5})$

(v) Circuit of Figure 7 (resistor)

$$I_1 = g_{m1}(V_1 - V_2) + y_A V_1, \quad (21)$$

$$I_2 = -g_{m1}(V_1 - V_2) + y_B V_2, \quad (22)$$

where $y_A = g_{N1} + s(C_{+1} + C_{N1})$,

$y_B = g_{P1} + s(C_{-1} + C_{P1})$

It should be noted that the terms of y_A, y_B and y_C are effective at very high frequency and selection of C_1 and C_2 in terms of y_{CT1} and y_{CT2} is quite large as compared with the parasitic capacitances, theirs effects are negligible. To decrease the effect of parasitic conductances of y_{CT1} and y_{CT2}, the proposed negative resistor is connected in parallel with the external capacitor. The low frequency range of proposed circuits can be extended.

3. Simulations and Discussions

To verify the performances of the proposed floating immittance function simulator circuits of Figures 3 – 7, the transistors of the transconductor using TSMC 0.18 μm technology has been simulated by the SPICE program with ±0.75 V supply voltage [12]. The aspect ratios of NMOS and PMOS transistors are selected as $L_N = L_P$ = 0.54 μm, W_N = 3.6 μm and W_P = 9 μm.

To demonstrate the electronic tunning feature of the proposed circuits in Figures 3 to 7, theirs components were selected as follows:

(i) Inductor using C_1 = 25 pF, $I_{01} = I_{02} = I_0$ = 50 μA, 100 μA and 200 μA,

(ii) Capacitor using C_1 = 25 pF, I_{01} = I_{03} = I_0 = 50μA, 100μA, 200 μA and I_{02} = I_{04} =100 μA,

(iii) FDNC using C_1 = C_2 = 25 pF, I_{01} = I_{02} = I_{03} = I_0 = 50μA, 100μA and 200 μA,

(iv) FDNR using C_1 = C_2 = 25 pF, I_{01} = I_{03} = I_0 = 50μA, 100μA, 200 μA and I_{02} = I_{04} = I_{05} =100 μA and

(v) Resistor using I_{01} = I_0 = 50 μA, 100 μA and 200 μA.

Figures 9 to 13 show the frequency responses of impedances of inductance, capacitance, FDNC, FDNR and resistance with bias currents of the transconductors. It should be noted that the simulated and ideal responses of them agree very well in the frequency range of about 3 decades as shown in Figures 9 to10, 2 decades in Figure 11, 1 decade in Figure 12 and more than 8 decades in Figure 13.

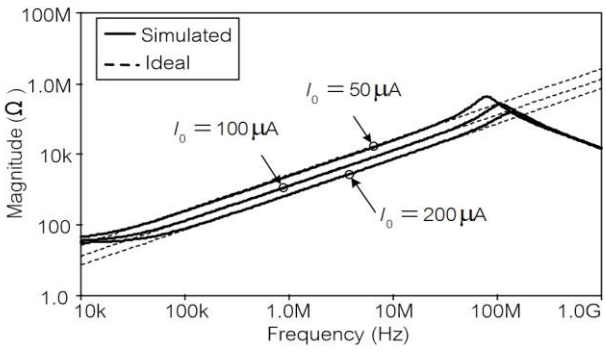

Figure 9 Frequency responses of the proposed Inductor with tunning of I_0.

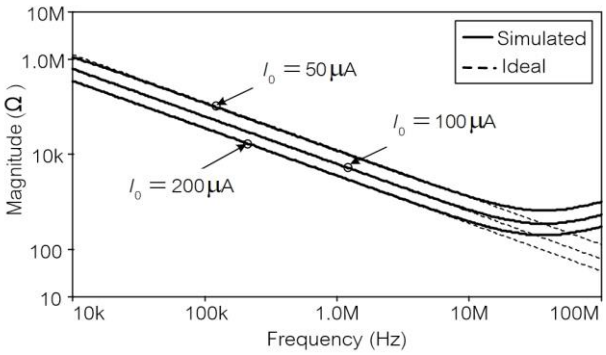

Figure 10 Frequency responses of the proposed capacitor with tunning of I_0.

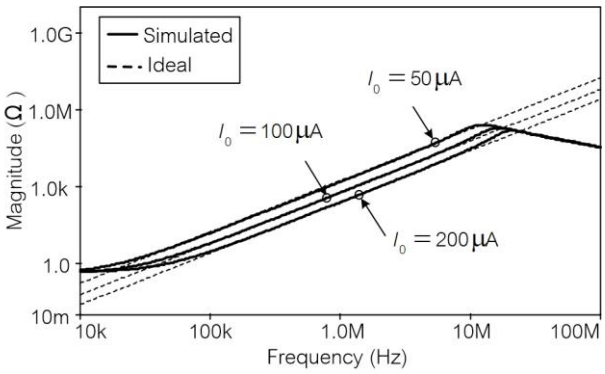

Figure 11 Frequency responses of the proposed FDNC with tunning of of I_0.

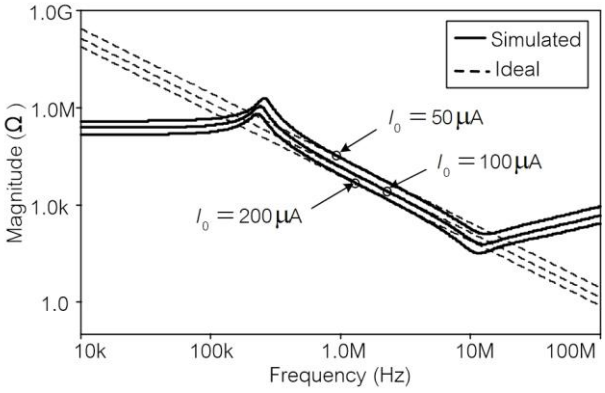

Figure 12 Frequency responses of the proposed FDNR with tunning of I_0.

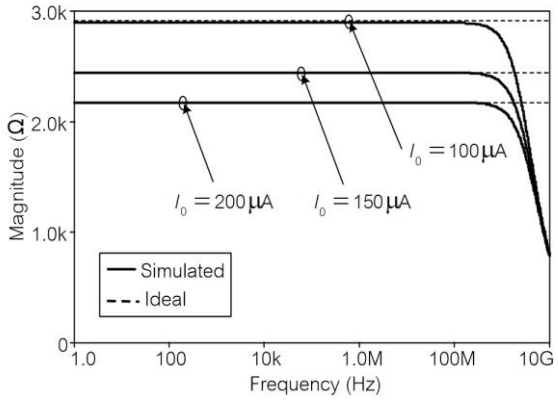

Figure 13 Frequency responses of the proposed resistor with tunning of I_0.

Figure 14 shows the simulated transient response of the proposed inductor for selecting its component as C_1 = 25 pF and I_{01} = I_{02} =180 μA and inputs of v_{in} = 200 mV and i_{in} = 79.5 μA at the frequency of 3 MHz. The components of the capacitor in Figure 4 are selected as C_1 = 25 pF, I_{01} = I_{03} = 200 μA and I_{02} = I_{04} = 100 μA, its transient response for inputs as v_{in} = 100 mV and i_{in} = 87 μA at the frequency of 3 MHz is displayed in Figure 15. The phase difference between v_{in} and i_{in} of these responses is approximate value of 89.77 degree. It is very close to the ideal of 90 degree.

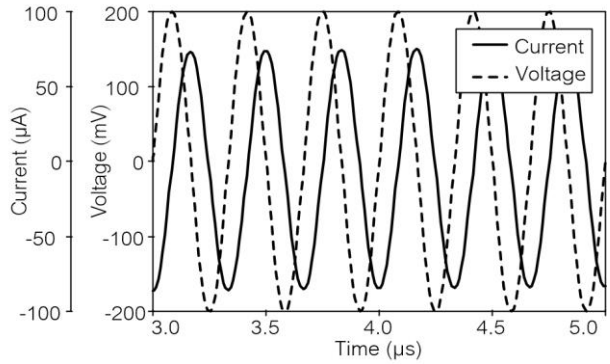

Figure 14 Transient response of the proposed inductor.

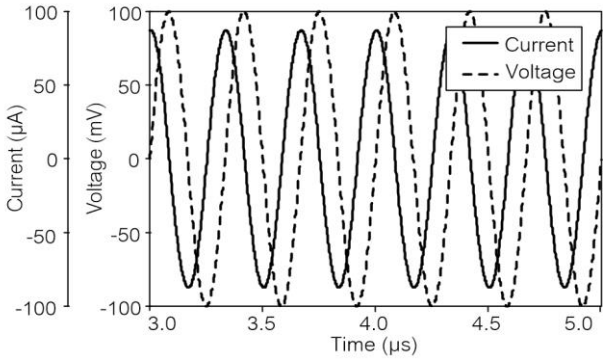

Figure 15 Transient response of the proposed capacitor.

To illustrate the applications of the proposed circuits, the proposed circuits of FDNC and FDNR are applied in the band-pass filter at center frequency of 2.2 MHz as shown in Figure 16 (a) and (b) using components as M_{eq} = 7.33 pF/s and D_{eq} = 3 aF·s, respectively. The proposed inductor, capacitor and resistor circuits using L_{eq} = 0.13 mH, C_{eq} = 40 pF and R_{eq} = 2.7 kΩ are designed in the RLC series resonant circuit as depicted in Figure 17.

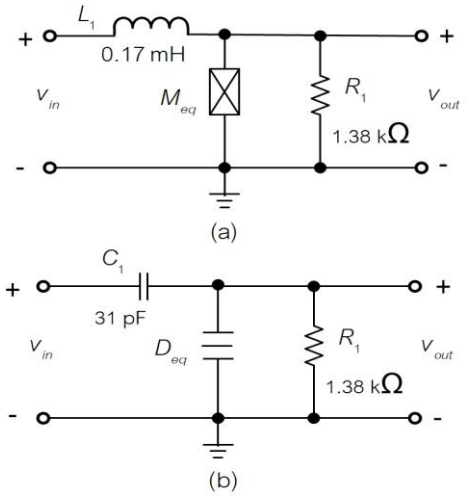

Figure 16 (a) Band-pass filter using proposed FDNC, (b) Band-pass filter using proposed FDNR.

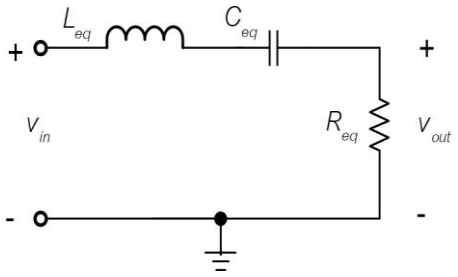

Figure 17 RLC resonant circuit using proposed circuits of Inductor and capacitor.

Figures 18 to 19 show the frequency responses of the band-pass filter of Figure 16 (a) and (b). It is noted that the simulated and ideal responses of these circuits are in good agreement. The deviations of them in the low- and high-frequency areas results from the parasitic elements of the transconductors.

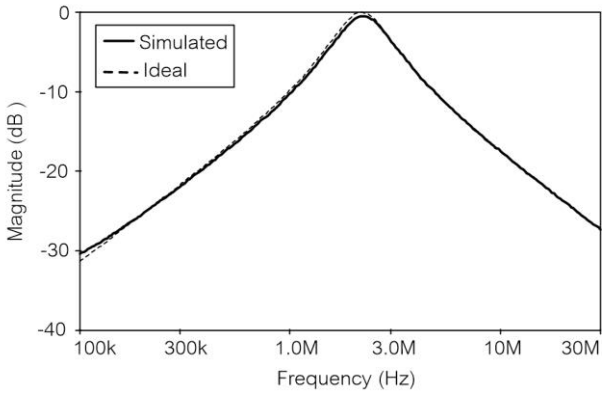

Figure 18 Frequency responses of the band-pass filter in Figure 16 (a).

The frequency response of the RLC resonant circuit of Figure 17 is presented in Figure 20, noted that its simulated result agrees well with ideal one.

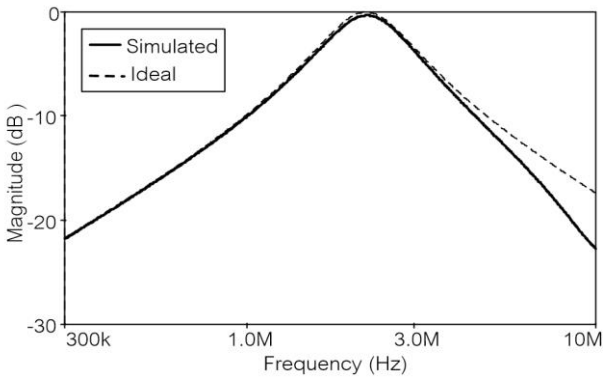

Figure 19 Frequency responses of the band-pass filter in Figure 16 (b).

In addition, Figure 21 shows the oscillator which is the application of the proposed negative resistor in RLC parallel resonant circuit using L_{eq} = 0.13 mH, C_{eq} = 40 pF and R_{eq} = R_1 = 2.7 kΩ. The transient response of the circuit is shown in Figure 22.

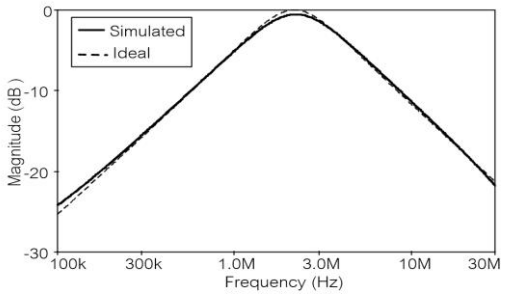

Figure 20 Frequency responses of the RLC resonant circuit in Figure 17.

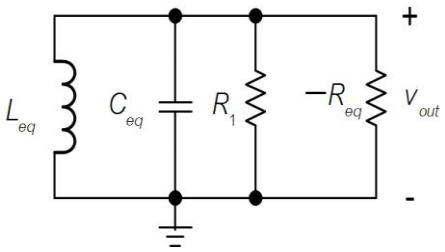

Figure 21 Oscillator using RLC resonant circuit and proposed negative resistor.

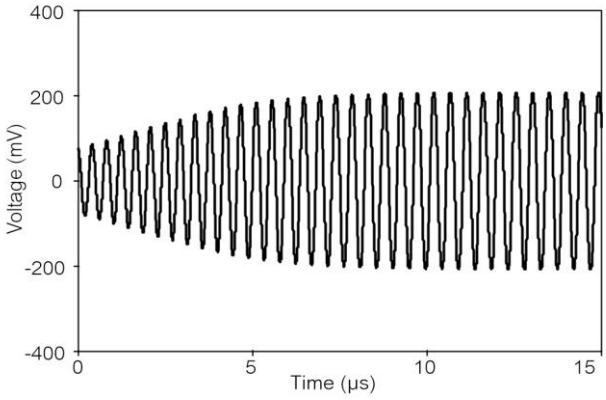

Figure 22 Transient response of the circuit in Figure 21.

4. Conclusion

Simple tunable floating immittance function simulators have been proposed. These circuits employ simple transconductor and only grounded capacitor. They provide attractive features of simple structure, low-component count, electronic tunability and suitable for integrated circuit implementation. The simulation results have been shown that the performances of the proposed circuits and theirs applications in band-pass filters and resonant circuits agree well with theoretical prophecy.

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